REMARKS

I. Status of the Claims

Claims 1 - 20 have been examined and stand rejected on various grounds. Claim 4 has been amended.

II. Rejections Under 35 U.S.C. §112

The Office Action identified a rejection to claim 4 under 35 U.S. C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the word "inputs" was mistakenly omitted from the claim. Claim 4 has been amended for the sole reason of adding the word "inputs" to complete the claim.

III. Rejections Under 35 U.S.C. §103

The Office Action identified rejections to claims 1 through 20 under 35 U.S.C. 103 as being unpatentable over Sartschev et al. (U.S. Patent No. 6,073,259) in view of Chu (U.S. Patent No. 4,164,648) and Murakami (U.S. Patent No. 5,872,745).

A) Claims 1, 9-10, 12 and 18-19

The office Action rejected these claims based on the argument that Sartschev discloses all of the claimed limitations except for the second plurality of delay elements and the coincidence circuit. The Office Action further reasons that Chu discloses the second plurality of delay elements, and Murakami discloses the coincidence circuit. Combining the three references allegedly renders the noted claims obvious.

It's important to understand the claimed subject matter in order to fully appreciate the fundamental differences between the claimed timing measurement circuit, and the cited art.

1) Claim 1

Claim 1 is directed to a time measurement circuit that has a first delay chain of delay elements, and a second delay chain of delay elements. A clock provides the input

for the first chain, while a stop signal provides the input for second delay chain. A coincidence circuit coupled to both of the delay chains produces an output representing the coincidence between the respective delay chain signals. This coincidence output reflects a time measurement.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

In contrast to the time measurement circuit claimed in claim 1, Sartschev describes using ***timing generation circuitry*** in automatic test equipment (ATE). Timing generators enable the creation of test signals that occur at a specified point in time with respect to a timing reference. Nowhere does Sartschev describe or suggest timestamp circuitry for making time measurements.

Chu describes a pair of start/stop oscillators that provide a way to measure a timing interval based on an oscillation frequency. The phase-locked oscillators of Chu do not provide access to each output of the delay chains (the claimed "taps" of the first delay chain). Because Chu does not create delayed edges from each of the taps that are fed into a coincidence circuit, it has little relevance to the subject matter of claim 1.

The Murakami patent discloses a counter-based time measurement scheme. The relevant portion of the patent cited by the Examiner, the coincidence circuit 112 of Figure 12, illustrates a correction scheme to correct for counter errors during the measurement. It does not disclose any couplings to delay chain taps (as claimed in claim 1), and does not suggest any form of output representative of the coincidence between one of the taps and one of the outputs of the second plurality of delay elements. Similar to the previously identified patents, Murakami has little relevance to the claimed subject matter of claim 1.

In short, the Office Action has identified references that allegedly illustrate a first delay chain (Sartschev), a second delay chain (one of the oscillator circuits of Chu), and a coincidence circuit (Murakami). By merely throwing these structures together, without regard to the claimed cooperation of the inputs and outputs of claim 1, the Office Action alleges that claim 1 is obvious. In other words, even if Sartschev, Chu and Murakami are combined, the combination still fails to disclose or remotely suggest most of the claimed features of claim 1.

For instance, none of the references disclose the second plurality of delay elements, wherein each of the delay elements is coupled to a STOP input. Moreover, none of the references alone or in combination disclose the coincidence circuit having the first plurality of inputs coupled to the first delay chain taps, and the second plurality of inputs coupled to each of the second delay chain delay elements. For these reasons, claim 1 is believed allowable over the cited art. Reconsideration is respectfully requested.

2) Claim 9

Claim 9 recites a counter having a count input and an input for disabling counting coupled to the STOP input. The Office Action fails to identify which of the three cited references allegedly discloses this feature, but a review of all three confirms that none of the cited references disclose it.

3) Claim 10

Claim 10 recites that each of the elements in the delay chain has a nominal delay of D and the difference between the longest delay and the shortest delay introduced by the second plurality of delay elements exceeds D. Again, a review of all three cited references fails to disclose or suggest any feature remotely similar to that claimed in claim 10.

4) Claim 12

Claim 12 is similar to claim 1, but recites first and second circuits that each have a plurality of outputs representing, respectfully, a delayed clock and a delayed STOP signal at each output. A third circuit accepts the outputs from the first and second circuits to

produce a digital output representative of the coincidence between one of the first plurality of signals and one of the second plurality of signals.

Similar to the arguments presented for claim 1, Chu's oscillator-based frequency measurement technique teaches against the claimed delay-tapping scheme, such that there would be no motivation whatsoever to combine the cited references. Reconsideration is requested.

5) Claim 18

Claim 18 depends from claim 12 and recites an intended use within the field of automatic test equipment. Chu and Murakami do not relate to ATE. Claim 18 also recites a duplicate time measurement circuit in addition to that recited in claim 12, such that both are coupled to a common clock. Nowhere is this described or remotely suggested in any of the cited references. Reconsideration is respectfully requested.

6) Claim 19

Claim 19 depends from claim 18 and recites an additional feature comprising a counter in each time measurement circuit coupled to the common clock. Like the features of claim 18, this too is not disclosed or suggested in the cited references.

B) Claims 2 - 5 and 14

The Examiner rejected these claims based on an argument that Murakami discloses the coincidence circuit utilizing a plurality of column circuits and logic circuits comparing the outputs connected to the taps to reflect coincidence of inputs.

These claims recite various features that provide for a two-dimensional array of samplers to reduce signal path delays associated with time stamp measurements. Specifically, the delayed edges from the delay chains are fed into the two-dimensional array of sampling latches to get a time measurement by finding out which sampled time of the N by M sampled times the transition took place.

While Murakami discloses what it identifies as a "coincident" circuit, it does not employ inputs and produce an output as claimed. Specifically, with respect to claim 2, Murakami's coincidence circuit does not have any column circuits (to thus form the array referred to above) having inputs coupled to any taps from a first delay chain of delay elements.

Likewise, with respect to claim 3, Murakami fails to disclose or suggest the claimed logic circuits, and the recited input and output couplings.

Claims 4, 5 and 14 recite an encoder feature for the column circuits that also is nowhere mentioned in Murakami, nor in any of the other references for that matter. Reconsideration is respectfully requested.

C) Claims 6 - 7

The Office Action rejected claims 6 - 7 based on the argument that Murakami discloses the use of a comparison circuit to compare the outputs of delay elements. This is inaccurate. While a comparison circuit is identified in Murakami, it does not compare the outputs of delay elements. It compares the outputs from high-speed counters, not the outputs from delay elements (ref. Figure 13). Moreover, claims 6 and 7 recite circuitry that produces intermediate signals. There is no language referring to comparison circuitry. For these reasons, claims 6 and 7 distinguish over the cited references.

D) Claims 8 and 15

Claims 8 and 15 were rejected based on the Sartschev reference because it discloses a calibration register. However, as noted above, claims 1 and 12 distinguish over Sartschev and the rest of the cited art for various reasons. Because claims 8 and 15 depend indirectly from claims 1 and 12, respectively, these claims are believed allowable over the cited art.

E) Claims 11 and 13

Claims 11 and 13 depend directly from claims 1 and 12, and were rejected based on the Sartschev reference because it discloses use of a delay-locked-loop in the delay chain. Noticeably absent is any comment from the Examiner concerning the continued motivation to employ Chu's oscillator scheme mixed in with the claimed delay lock loop. That's because there is none. Teaching the use of oscillators (included in, for example a phase-locked loop) is fundamentally different than the use of delay locked loops. Reconsideration is requested.

F) Claims 16, 17 and 20

Claims 16, 17 and 20 were rejected based on the portion of Sartschev that discloses implementation of a timing generator on a CMOS chip. Sartschev does not disclose the timing measurement circuit of claim 12 implemented on a CMOS chip. Therefore, for all the reasons applicable to the patentability of claim 12, claims 16, 17 and 20 are also patentable over the cited art.

Please charge a two-month extension of time in the amount of $420 to Deposit Account No. 20-0515.

Respectfully Submitted

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